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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/646,478
Filing Date: August 22, 2003
Appellant(s): KAWAGOE, DAISUKE

MAILED
AUG 0 9 2007
GROUP 2800

Andrew Peret
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed June 7, 2007 appealing from the Office action mailed March 21, 2006.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

The examiner is not aware of any related appeals, interferences, or judicial proceedings, which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings, which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

6,810,583	Carpenter et al.	11/2004
6,531,661	Uchikawa et al.	3-2003
6,534,723	Asai et al.	3-2003

Appendix "A", marked up figure 6 of Carpenter et al., US Patent No. 6,810,583

Appendix "B", marked up figure 7 of Carpenter et al., US Patent No. 6,810,583

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 40-44 rejected under 35 U.S.C. 102(e) as being anticipated by Carpenter (US Patent No. 6,810,583).

Regarding claim 40, Carpenter, in figure 6, discloses a substrate comprising: a first dielectric layer (D1, as marked up on figure 6 in appendix "A"); a second dielectric layer (D2, as marked up on figure 6 in appendix "A"); a first conductive layer (C1, as marked up on figure 6 in appendix "A"); between the first and second dielectric layers; a third dielectric layer (D3, as marked up on figure 6 in appendix "A"); the second dielectric layer being between the first and third dielectric layers; a second conductive layer (C2, as marked up on figure 6 in appendix "A"); between the second dielectric layer and the third dielectric layer, the second conductive layer including a first skip via (57) that extends through the first and second dielectric layers; and a third conductive layer (C3) on the third dielectric layer, the third conductive layer including a second via (26) that extends through the third dielectric layer, the second via and the first skip via being stacked on top of one another (see marked up figure 6 in appendix "A").

Regarding claim 41, Carpenter further discloses the first skip via includes a longitudinal axis (longitudinal axis passing through the first skip via, see marked up in figure 6, in appendix "A") and the second via includes a longitudinal axis (longitudinal axis passing through the second via, see marked up in figure 6, in appendix "A"), the longitudinal axis of the first skip via being substantially aligned with the longitudinal axis of the second via (see marked up in figure 6, in appendix "A").

Regarding claim 42, Carpenter further discloses the first, second and third dielectric layers are formed on a core (C5, see marked up in figure 6, in appendix "A").

Regarding claim 43, Carpenter further discloses a fourth conductive layer (C4, see marked up in figure 6, in appendix "A") between the first dielectric layer and the core.

Regarding claim 44, Carpenter further discloses the first, second and third conductive layers are patterned conductive layers (see figure 6).

Claims 47-51 rejected under 35 U.S.C. 102(e) as being anticipated by Carpenter (US Patent No. 6,810,583).

Regarding claim 47, Carpenter, in figure 7, discloses a substrate comprising: a first dielectric layer (D1, marked up on figure 7 in appendix "B"); a second dielectric layer (D2, marked up on figure 7 in appendix "B"); a first conductive layer (C2, marked up on figure 7 in appendix "B") between the first and second dielectric layers; a third dielectric layer (D3, marked up on figure 7 in appendix "B"), the second dielectric layer being between the first and third dielectric layers; a second conductive layer (C3, marked up on figure 7 in appendix "B") between the second and third dielectric layers, the second conductive layer including a first skip via (V1, marked up on figure 7 in appendix "B") that extends through the first and second dielectric layers; a fourth dielectric layer (D4, marked up on figure 7 in appendix "B"), the third dielectric layer being between the second and fourth dielectric layers; a third conductive layer (C4,

marked up on figure 7 in appendix "B") between the third and fourth dielectric layers; and a fourth conductive layer (C5, marked up on figure 7 in appendix "B") on the fourth dielectric layer, the fourth conductive layer including a second skip via (V2, marked up on figure 7 in appendix "B") that extends through the third and fourth dielectric layers, the second skip via and the first skip via being stacked on top of one another (see marked figure 7 in appendix "B").

Regarding claim 48, Carpenter further discloses the first skip via and the second skip via each include a longitudinal axis (longitudinal axis of axis of firs skip via and second skip via), the longitudinal axis of the first skip via being substantially aligned with the longitudinal axis of the second skip via (see marked up figure 7 in appendix "B").

Regarding claim 49, Carpenter further discloses the first, second, third and fourth dielectric layers are formed on a core (C7, as marked up on figure 7 in appendix "B").

Regarding claim 50, Carpenter further discloses a fifth conductive layer (C6, marked up on figure 7 in appendix "B") between the first dielectric layer and the core.

Regarding claim 51, Carpenter further discloses the first, second, third and fourth conductive layers are patterned conductive layers (see figure 7).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 54-56 are rejected under 35 U.S.C. 103(a) as being unpatentable over Carpenter, as applied to claim 47 above.

Regarding claim 54, Carpenter discloses all the features of the claimed invention as applied to claim 47 above, including a fifth dielectric layer (D5, marked up on figure 7 in appendix "B"), the fourth conductive layer (C5, marked on figure 7 in appendix "B") being between the fourth and fifth dielectric layers; a sixth dielectric layer (D6, marked up on figure 7 in appendix "B"), the fifth dielectric layer being between the fourth and sixth dielectric layers; a fifth conductive layer (C6, marked up on figure 7 in appendix "B") between the fifth and sixth dielectric layers; a sixth conductive layer (C7, marked up on figure 7 in appendix "B") on the sixth dielectric layer. Carpenter further discloses a third sip via (V3, marked up on figure 7 in appendix "B"), a third skip via that extends through the fifth and sixth dielectric layers, but does not disclose the sixth conductive layer including connected to the third skip via. However, as can be seen at various places in the figure, the conductor layer / patterns are connected to the via

depending upon the desired electrical connection for signal, power or ground connections.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to provide the circuit board of Carpenter with the third skip via connected to the sixth conductive layer, in order to have desired electric connection for signal, power or ground.

Regarding claim 55, Carpenter further discloses the first, second and third skip vias each include a longitudinal axis, the longitudinal axis of the first skip via being substantially aligned with the longitudinal axis of the second and third skip vias (see marked up figure 7 in appendix "B").

Regarding claim 56, Carpenter further discloses the first, second, third, fourth, fifth and sixth conductive layers are patterned conductive layers (see figure marked up figure 7 in appendix "B").

Claims 45-46, 52-53 and 57-58 are rejected under 35 U.S.C. 103(a) as being unpatentable over Carpenter as applied to claims 40, 47 and 54 above, and further in view of Uchikawa (US Patent No. 6,531,661) and Asai (US Patent No. 6,534,723).

Regarding claim 45, Carpenter discloses all the features of the claimed invention as applied to claim 40 above, including the first skip via and second via, but does not disclose the first skip via has a diameter between 49 μm and 85 μm and the second via has a diameter between 49μm and 85μm. However, the size of the via will depend upon various factor such as the method of making the via, the thickness of the dielectric material and in particular the required current carrying capacity for minimum loss through the via.

Uchikawa discloses printed circuit board with via diameter of 30 to 200 μm and a depth of 0.05 to 0.5 mm (column 4, line 60-64).

Asai discloses a circuit board with the insulative substrate with about 20 to 600 μm to assure a sufficient insulation performance with the diameter of holes within a range of 50 to 200 μm, to facilitate filling of conductive material to have reliable electrical connection (column 11, line 66 to column 12, line 18).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to provide the circuit board of Carpenter with the first skip via having a diameter between 49 μm and 85 μm and the second via having a diameter between 49μm and 85μm, as taught by Uchikawa and Asai, in order to have desired current carrying capacity.

Further, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involve only routine skill in the art. *In re Aller*, 105 USPQ 233.

Regarding claim 46, Carpenter discloses all the features of the claimed invention as applied to claim 40 above, including the first skip via and the second via, but does not disclose the first skip via has a length between 58 μm and 92 μm and the second via has a length between 24μm and 36μm. However, the length of via will depend upon the thickness of the insulating layers of the circuit board and number of insulting board layers the via travels.

As applied to claim 45 above, Uchikawa discloses printed circuit board with via diameter of 30 to 200 μm and a depth of 0.05 to 0.5 mm (column 4, line 60-64). Also, Asai discloses a circuit board with the insulative substrate with about 20 to 600 μm to assure a sufficient insulation performance with the diameter of holes within a range of 50 to 200 μm, to facilitate filling of conductive material to have reliable electrical connection (column 11, line 66 to column 12, line 18).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to provide the circuit board of Carpenter with via lengths of both the vias as claimed, as taught by Asai and Uchikawa, in order to have electrical connection between the different layers of the circuit board for transmitting signals.

Regarding claim 52, Carpenter discloses all the features of the claimed invention as applied to claim 47 above, including the first skip via and the second skip via, but does not discloses the first skip via has a diameter between 49 μm and 85 μm and the second skip via has a diameter between 49μm and 85μm. However, the size of the via will depend upon various factor such as the method of making the via, the

thickness of the dielectric material and in particular the required current carrying capacity for minimum loss through the via.

Uchikawa discloses printed circuit board with via diameter of 30 to 200 μm and a depth of 0.05 to 0.5 mm (column 4, line 60-64).

Asai discloses a circuit board with the insulative substrate with about 20 to 600 μm to assure a sufficient insulation performance with the diameter of holes within a range of 50 to 200 μm, to facilitate filling of conductive material to have reliable electrical connection (column 11, line 66 to column 12, line 18).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to provide the circuit board of Carpenter with the first skip via having a diameter between 49 μm and 85 μm and the second skip via having a diameter between 49μm and 85μm, as taught by Uchikawa and Asai, in order to have desired current carrying capacity.

Further, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involve only routine skill in the art. *In re Aller*, 105 USPQ 233.

Regarding claim 53, Carpenter discloses all the features of the claimed invention as applied to claim 47 above, including the first skip via and the second skip via, but does not disclose both skip via has a length between 58 μm and 92 μm. However, the length of via will depend upon the thickness of the insulating layers of the circuit board and number of insulting board layers the via travels.

As applied to claim 52 above, Uchikawa discloses printed circuit board with via diameter of 30 to 200 μm and a depth of 0.05 to 0.5 mm (column 4, line 60-64). Also, Asai discloses a circuit board with the insulative substrate with about 20 to 600 μm to assure a sufficient insulation performance with the diameter of holes within a range of 50 to 200 μm, to facilitate filling of conductive material to have reliable electrical connection (column 11, line 66 to column 12, line 18).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to provide the circuit board of Carpenter with via lengths of both the vias as claimed, as taught by Asai and Uchikawa, in order to have electrical connection between the different layers of the circuit board for transmitting signals.

Regarding claim 57, Carpenter discloses all the features of the claimed invention as applied to claim 54 above, including the first skip via and the second skip via and the third skip via but does not disclose each via has a diameter between 49 μm and 85 μm. However, the size of the via will depend upon various factor such as the method of making the via, the thickness of the dielectric material and in particular the required current carrying capacity for minimum loss through the via.

Uchikawa discloses printed circuit board with via diameter of 30 to 200 μm and a depth of 0.05 to 0.5 mm (column 4, line 60-64).

Asai discloses a circuit board with the insulative substrate with about 20 to 600 μm to assure a sufficient insulation performance with the diameter of holes within a

range of 50 to 200 μm, to facilitate filling of conductive material to have reliable electrical connection (column 11, line 66 to column 12, line 18).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to provide the circuit board of Carpenter with each skip via having a diameter between 49 μm and 85 μm, as taught by Uchikawa and Asai, in order to have desired current carrying capacity.

Further, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involve only routine skill in the art. *In re Aller*, 105 USPQ 233.

Regarding claim 58, Carpenter discloses all the features of the claimed invention as applied to claim 54 above, including the first skip via, the second skip via and the third skip via but does not disclose the skip vias have a length between 58 μm and 92 μm. However, the length of via will depend upon the thickness of the insulating layers of the circuit board and number of insulting board layers the via travels.

As applied to claim 52 above, Uchikawa discloses printed circuit board with via diameter of 30 to 200 μm and a depth of 0.05 to 0.5 mm (column 4, line 60-64). Also, Asai discloses a circuit board with the insulative substrate with about 20 to 600 μm to assure a sufficient insulation performance with the diameter of holes within a range of 50 to 200 μm, to facilitate filling of conductive material to have reliable electrical connection (column 11, line 66 to column 12, line 18).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to provide the circuit board of Carpenter with via lengths of all the skip vias as claimed, as taught by Asai and Uchikawa, in order to have electrical connection between the different layers of the circuit board for transmitting signals.

(10) Response to Argument

NOTE: Clarification for the marked up figures: This is for better understanding the marked up copy of figure 6 and 7 (appendix A and B) of prior art to Carpenter (US Patent No. 6,810,583). These remarks were enclosed as an "*Attachment to Notice of Panel Decision From Pre-Appeal Brief Review*" mailed on March 5, 2007.

Regarding figure 6 (Appendix A).

C1, C2, C3, C4, C5, as marked up on the figure is indicating a conductive layer on the surface of the dielectric layer and not only the element pointed by the arrow.

Regarding figure 7 (Appendix B).

C1, C2, C3, C4, C5, C6, C7, as marked up on the figure is indicating a conductive layer on the surface of the dielectric layer and not only the element pointed by the arrow.

(A) Appellant's argument for the rejection of claims 40-44 under 35 USC 102(e) by Carpenter et al., states that conductor layer C2 and via as shown on marked up

drawing (figure 6) are separate entity and are shown with separate cross-hatching pattern. Therefore, Carpenter does not teach or suggest **"the second conductive layer including a first skip via that extend trough the first and second dielectric layers"** as recited in claim 40.

This not found to be persuasive.

As clearly shown in the marked up figure (6, appendix "A"), via (57) is a skip via passing through first (D1) and second (D2) dielectric layers and in direct contact with the second conductor layer (C2). Therefore, the structure of Carpenter as shown in marked up figure (6) shows **"the second conductive layer (C2) including a first skip via (57) that extend through the first (D1) and second (D2) dielectric layers"** as recited in the claim. This is a structural claim and figure (6) as explained, discloses the final structure as recited in the claim. Different cross hatching pattern identifies the conductor layer and the via, but as a whole discloses the structure as recited in the claim. Therefore, Carpenter et al. meets the limitation.

Appellant further argues that conductor layer (C3, marked up figure 6) does not include any vias. The vias and the conductor layer are shown as separate entity. Therefore, Carpenter does not teach or suggest **"the third conductive layer including a second via that extends through the third dielectric layer"** as recited in claim 40.

This not found to be persuasive.

As clearly shown in the marked up figure (6, appendix "A"), via (26) pass through the dielectric layer (D3) and in direct contact with the conductor layer (C3). Therefore, the structure of Carpenter as shown in marked up figure (6) shows **"the third**

conductive layer (C3) including a second via (26) that extends through the third dielectric layer" as recited in the claim. This is a structural claim and figure (6, marked up), as explained, discloses the final structure as recited in the claim. Different cross hatching pattern identifies the conductor layer and the via, but as a whole discloses the structure as recited in the claim. Therefore, Carpenter et al. meets the limitation.

(B) Appellant's argument for the rejection of claims 47-51 under 35 USC 102(e) by Carpenter et al., states that the examiner's marked up figure (7) shows that conductive layer (C3) does not include any vias. Each via is shown as a separate entity from metallization and shown with separated cross-hatching pattern. Therefore, Carpenter does not teach or suggest **"the second conductive layer including a first skip via that extends through the first and second dielectric layers"** as recited in claim 47.

This not found to be persuasive.

As clearly shown in the marked up figure (7, appendix "B") the first skip via (V1) extend through the first (D1) and second (D2) dielectric layers and is in direct contact with the second conductive layer (C3). This is a structural claim and the figure (7, marked up), as explained, discloses the final structure as recited in the claim. Therefore, Carpenter discloses, **"the second conductive layer (C3) including a first skip via (V1) that extends through the first (D1) and second (D2) dielectric layers"**. Different cross hatching pattern identifies the conductor layer and the via, but as a

whole discloses the structure as recited in the claim. Therefore, Carpenter et al. meets the limitation.

Appellant further argues that conductor layer (C5, marked up figure 7) does not include any vias. The via is shown as a separate entity from the conductor layer and with separate cross-hatching patterns. Therefore, Carpenter does not teach or suggest **"the fourth conductive layer including a second skip via that extends through the third and fourth dielectric layers"** as recited in claim 47.

This not found to be persuasive.

As clearly shown in the marked figure (7, appendix "B") the second skip via (V2) extends through the third (D3) and fourth (D4) dielectric layers and in direct contact with the fourth conductive layer (C5). This is a structural claim and the figure (7, marked up), as explained, discloses the final structure as recited in the claim. Therefore, Carpenter discloses **"the fourth conductive layer (C5) including a second skip via (V2) that extends through the third (D3) and fourth (D4) dielectric layers"** as recited in the claim. Different cross hatching pattern identifies the conductor layer and the via, but as a whole discloses the structure as recited in the claim. Therefore, Carpenter et al. meets the limitation.

(C) Appellant's argument for the rejection of dependent claims 54-56 under 35 USC 103 (a) by Carpenter et al., and claims 45, 46, 53, 57, by Carpenter in view of Uchikawa and Asai, states that those claims depend (directly or indirectly) upon the

independent claims 40 and 47, and incorporate all of the limitation of claims 40 and 47, should be allowable for the reason provided above with respect to claims 40 and 47.

This is not found to be persuasive.

As explained above, the prior art of Carpenter discloses the structure as recited in independent claims 40 and 47. Therefore the arguments are moot.

Further, Appellant states that the office must provide specific, objective evidence of record for a finding of a suggestion or motivation to combine reference teachings and must explain the reasoning by which the evidence is deemed to support such a finding and the examiner must avoid hindsight.

This is not found to be persuasive.

Though, the examiner recognizes that references cannot arbitrarily be combined and there must be some reason why one skilled in the art would be motivated to make the proposed combination of primary and secondary references, there is no requirement that a motivation to make the modification be expressly articulated. The test for combining references is what the combination of disclosures taken, as a whole would suggest to one of ordinary skill in the art.

Further, any judgment on obviousness is in a sense necessarily a reconstruction based on hindsight reasoning, but so long as it takes into account only knowledge which was within the level of ordinary skill in the art at the time the claimed invention was made and does not include knowledge gleaned only from applicant's disclosure, such a reconstruction is proper." *In re McLaughlin* 443 F.2d 1392, 1395, 170 USPQ 209, 212 (CCPA 1971).

In this case the primary reference discloses the substrate structure with conductor layers, dielectric layers, the via and skip via. Providing additional conductive layer and vias, as recited in the dependent claims, would be obvious to a person ordinary skill in the art to increase the wiring density of the board. Similarly, changing the size of the via depending upon the method used, and current carrying capacity desired, would be obvious to a person of ordinary skill in the art.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Ishwar (I. B.) Patel

July 31, 2007

Conferees:

Darren Schuberg

Dean Reichard

IB Patel

Ishwar (I. B.) Patel

APPENDIX "A"

application # 10/646,478
AU : 2841

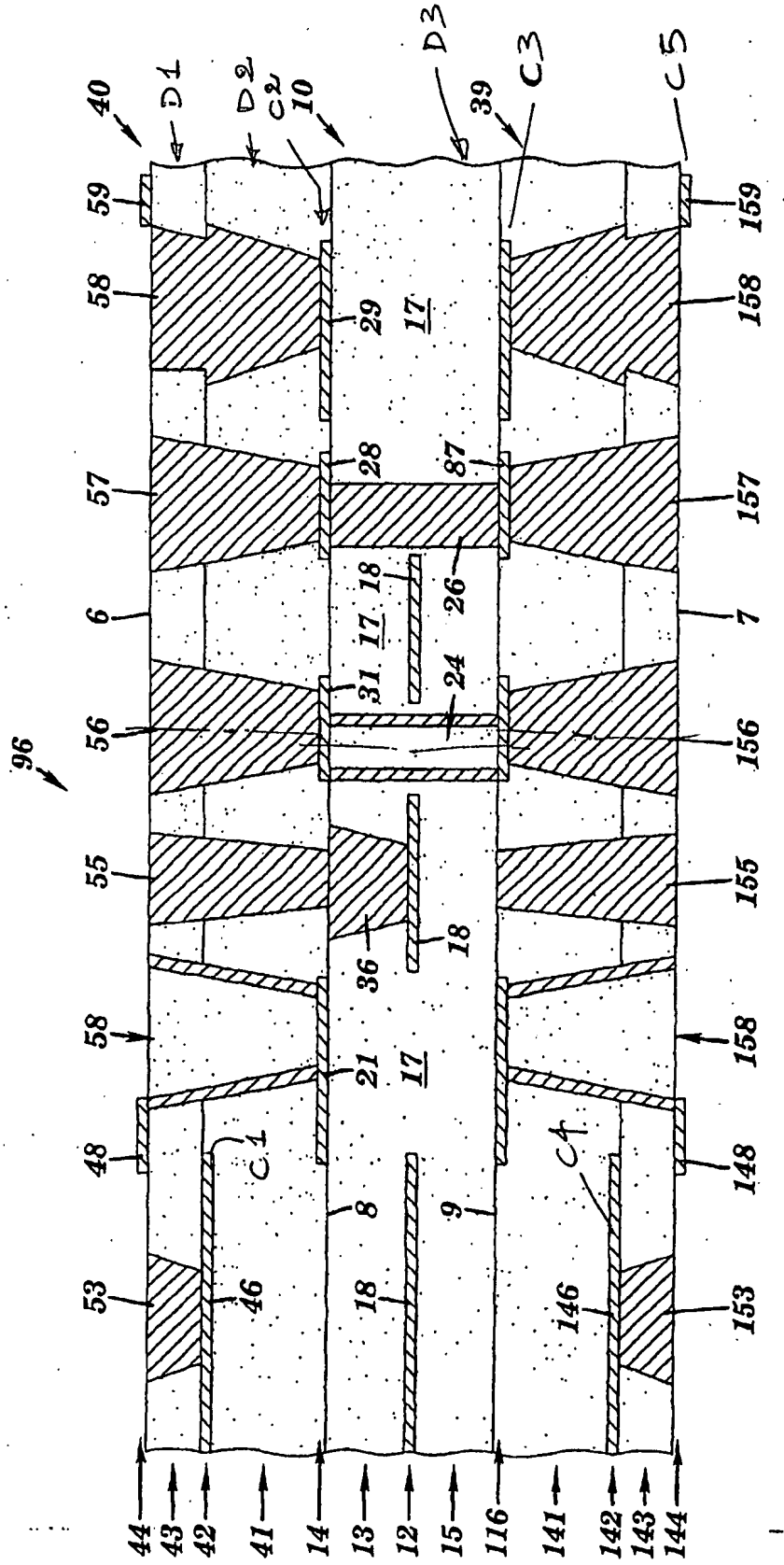

FIG. 6

IBalla

APPENDIX: "B"

application # 10/646,478
AU : 2841

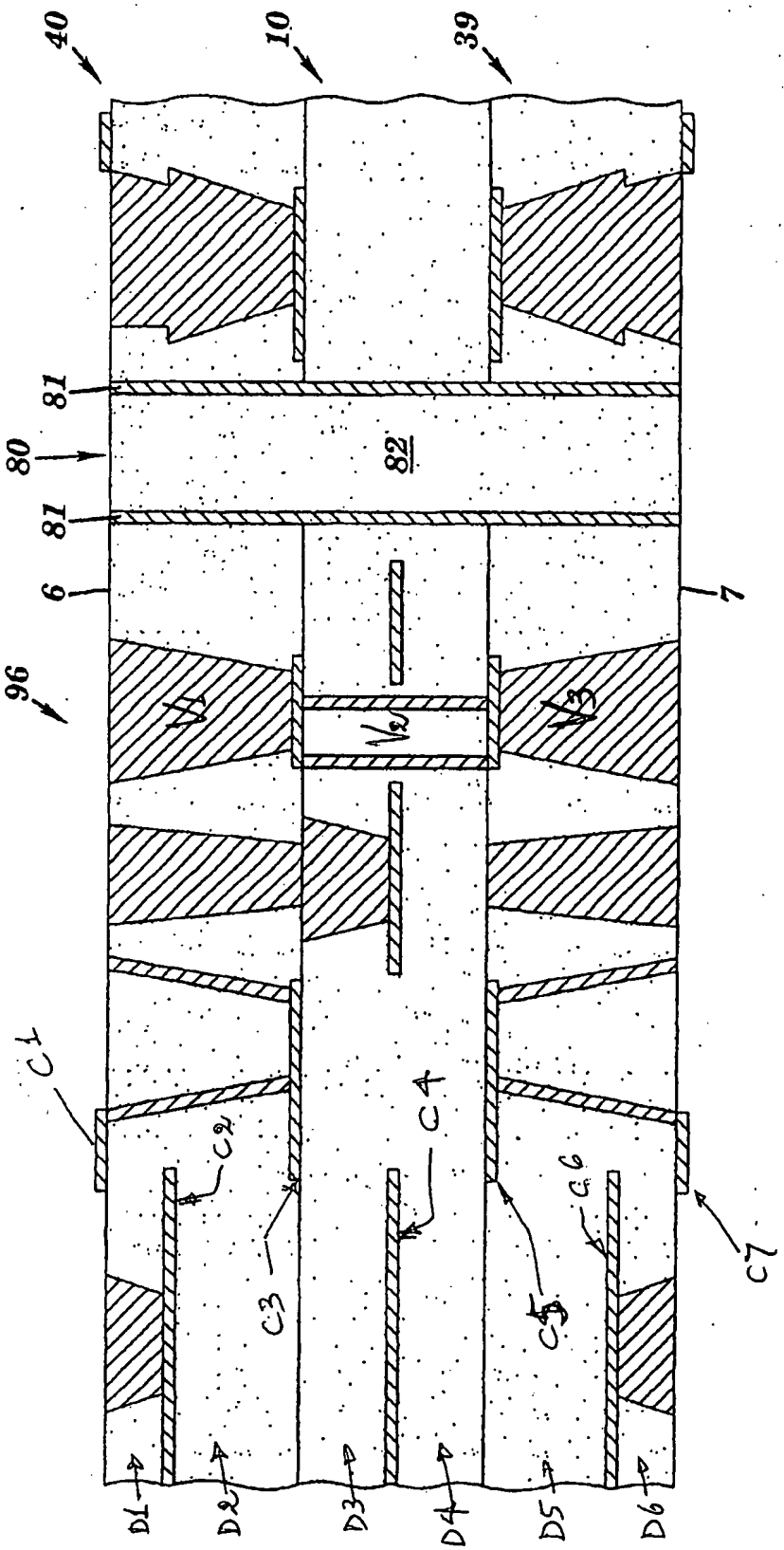

FIG. 7

IB Patel